Double Patenting Rejection

Claims 38-52, 54-59, and 62-79 were rejected under the judicially created doctrine of double patenting over claims 1-19 of U.S. Patent No. 5,923,584.

Applicant will provide a suitable Terminal Disclaimer when all claims are indicated to be otherwise allowable.

§103 Rejection of the Claims

Claims 38-52, 54-59, and 62-79 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Nihira et al. (U.S. Patent No. 4,908,324).

The Nihira et al patent relates to a method for making a bipolar transistor. The Office Action, in rejecting the claims under 35 U.S.C. § 103(a) only, concedes that Nihira et al does not show each and every element of the claims, arranged as shown in the claims. Although the Examiner contends in Paragraph 7 of the Office Action , without citation of authority, that such an interpretation "is contrary to the intent and purpose of an obvious type 103 rejection," MPEP Section 2143.03 states that in order to establish *prima facie* obviousness, "all the claim limitations must be taught or suggested by the prior art."

Applicant maintains that in considering the differences between what is shown in the cited Nihira patent and what Applicant claims, the question under 35 U.S.C. 103 is not whether those differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious. *Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 218 USPQ 871 (Fed. Cir. 1983); *Schenck v. Nortron Corp.*, 713 F.2d 782, 218 USPQ 698 (Fed. Cir. 1983); *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1143, 227 USPQ 543, 551 (Fed. Cir. 1985); MPEP § 2141.02. Applicant submits that the present office action fails to establish a *prima facie* case of obviousness of the claimed invention, taken as a whole, of the rejected claims. Since a *prima facie* showing of obviousness has not been established, Applicant has no burden of showing "criticality of the elements in order to satisfy the enablement requirement" as the Office Action contends in Paragraph 7.

The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). To do

that the Examiner must show that some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art would lead an individual to combine the relevant teaching of the references. *Id.* Applicant appreciates the fact that the Examiner has now cited three additional patents to show features not found in the Nihira which was to sole patent referred to in the original rejections. Applicant suggest however that in citing the additiopnal patents the Office Action has not shown a *prima facie* case of obviousness since no motivation to combine the disclosures has been provided and no indication has been given as to why there would be an expectation of success in combining the patents as the Office Action now suggests.

The previous Office Action took official notice that "the use of photoresist is well known in the art as a means of patterning structures in the semiconductor industry and would be obvious to form the resist, as recited, as part of a conventional multilevel interconnect process to enable formation of interconnects and bond pads necessary to incorporate the disclosed device in an integrated circuit" and now cites Schrantz et al 5,683,939 in support of that contention.

Schrantz et al deals with semiconductor devices having grown diamond insulation and passivation layers and with second level resistors. While Schrantz et al may indeed show the "use of photoresist for patterning", "the use of etch stop for stopping an etchant" and the "use of an etch stop in an etch back planarization process," the Office Action provides no rationale for combining Schrantz et al with the Nihira patent which forms the primary basis for the rejection. There is no reasoned indication in the Office Action as to why one of ordinary skill in the art would look to Schrantz et al for disclosure of photoresist techniques to modify the teachings of Nihira.

Additionally, the previous Office Action states: "Further, it would be obvious and is well known to use As as an N-type dopant" and now cites Shibib 5,541,429 as teaching that "arsenic is used to dope polysilicon to form a conductive material." The previous Office Action also took official notice that "As is well known as a dopant and it would have been obvious to switch the dopant types of the structure to provide greater process and device latitude" and the present Office Action says that the arsenic doping of Shibib "could be switched with other dopants" (citing col 5, ln 52-55, and col. 1, ln 38 thereof).

The cited Shibib patent relates to a vertical field-effect transistor with a laterally recessed channel region, a vertical field-effect transistor having a graded diffusion junction, a static random accessmemory cell having a vertical *n*-channel field-effect transistor and a vertical *p*-channel field-effect transistor and methods of forming them. While Shbib may indeed show the "that arsenic is used to dope polysilicon to form a conducting material" or "that arsenic could be switched with other dopants," the Office Action provides no rationale for combining Shibib with the Nihira patent which forms the primary basis for the rejection. There is no reasoned indication in the Office Action as to why one of ordinary skill in the art would look to Shibib for disclosure "that arsenic is used to dope polysilicon to form a conductive material" to somehow modify the teachings of Nihira.

Finally the previous Office Action further stated "...the use of Ti silicide as an etch stop material is also well known in the art and would be obvious to use in a conductive poly structure in order to both stop an etch and to further increase the conductivity of the structure." The present cites Kosa et al 5, 416, 736 as teaching "the use of titanium silicide as an etch stop layer, col. 10, ln. 42 - 44". While Kosa may indeed show the use of Ti silicide as an etch stop material when etching the first insulating layer 44 in Kosa, the Office Action provides no rationale for combining Kosa with the Nihira patent which forms the primary basis for the rejection. There is no reasoned indication in the Office Action as to why one of ordinary skill in the art would look to Kosa for disclosure of "...the use of Ti silicide as an etch stop material," to somehow modify the teachings of Nihira.

At a minimum, the Office Action also fails to show how Nihira,, which consistently shows a structure where neither polycrystalline silicon layer 11 nor silicon layer 9 has a thickness selected "such that the lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region" (a feature common to amended claims 38 - 45, 47 - 52 and their dependent claims 54 - 79)" where oxide region 8 extends above the upper surface of silicon layer 11. Claims 38 - 43, 45 and 48 - 52 have all been amended to more clearly distinguish from the cited Nihira patent by referring to the relationship of the lowest upper surface of the first silicon layer relative to the "oxide layer" rather than the "field oxide layer".

Claim 44 was not amended because it had already claimed the relation ship between the lowest upper layer of the first silicon layer and the oxide layer.

Applicant reserves the right to further demonstrate how the cited patents may not properly be combined to show what is claimed in claims 38-45, 47-52 and 54 - 79. Reconsideration and withdrawal of the improper rejection under 35 U.S.C. § 103 and allowance of the pending claims, as amended, is respectfully requested.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6970 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

MARTIN CEREDIG ROBERTS ET AL.

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Date September 5, 2002 By

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Box RCE, Commissioner of Patents, Washington, D.C. 20231, on this 5th day of September, 2002.

Amy Moriarty
Name

Signature

Docket No. [illegible]US6 Micron Ref. No. 93-0512.05
WD # 418539

CLEAN VERSION OF PENDING CLAIMS

METHOD FOR FORMING AN INTEGRATED CIRCUIT INTERCONNECT USING A DUAL POLY PROCESS
Applicant: Martin Ceredig Roberts et al.
Serial No.: 09/745,780

Claims 38-45, 47-52, 54-59, 62-65, and 68-79, as of September 5, 2002 (Date RCE filed with a Response to Final Office Action).

38. (Amended) An intermediate in the manufacture of a semiconductor interconnect overlying region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region; and

a second polycrystalline silicon layer overlying the first polycrystalline silicon layer and the first substrate region.

39. (Amended) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer; and

a second polycrystalline silicon layer overlying the etch stop layer and the first substrate region.

40. (Amended) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide] region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer; and

a second polycrystalline silicon layer overlying the etch stop layer and the first substrate region, the upper surface of the second polycrystalline silicon layer being substantially planar and aligned with the upper surface of the first polycrystalline silicon layer adjacent an interface between the first polycrystalline silicon layer and the second polycrystalline silicon layer such that the interface has no horizontal component.

D' cont.

41. (Amended) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

a field oxide region overlying at least a portion of the second substrate region;

a gate oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the field oxide and gate oxide regions but not the first substrate region and having a thickness selected such that the lowest upper surface of the first polycrystalline silicon layer is higher than the highest upper surface of the oxide regions;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer; and

a second polycrystalline silicon layer overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the first polycrystalline silicon layer and the second polycrystalline silicon layer.

42. (Amended) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

a polycrystalline silicon plug overlying the first substrate region and having the upper surface thereof aligned with an upper surface of the polycrystalline silicon layer adjacent the second substrate region such that a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug has no horizontal component; and

a photoresist mask of material resistant to polycrystalline silicon etching overlying the polycrystalline silicon plug and an adjacent portion of the first polycrystalline layer surrounding the polycrystalline silicon plug thereby defining an electrical interconnect.

43. (Amended) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

a polycrystalline silicon plug overlying the first substrate region and having an upper

surface thereof aligned with an upper surface of the polycrystalline silicon layer adjacent the second substrate region such that a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug has no horizontal component; and

a photoresist mask overlying the polycrystalline silicon plug to define an electrical interconnect.

45. (Amended) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a polycrystalline silicon plug overlying the first substrate region; and

a polycrystalline silicon layer overlying a portion of the oxide region adjacent the polycrystalline silicon plug, but not the first substrate region, the polycrystalline silicon layer having a thickness selected such that a lowest upper surface of the polycrystalline silicon layer is higher than a highest upper surface of the oxide region, the polycrystalline silicon layer also having an upper surface thereof in the region adjacent the polycrystalline silicon plug aligned with an upper surface of the polycrystalline silicon plug such that the vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug has no horizontal component.

47. An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

at least one oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying a portion of the oxide region adjacent the first substrate region, but not the first substrate region, and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer; and

a second polycrystalline silicon layer overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the first polycrystalline silicon layer and the second polycrystalline silicon layer.

48. (Amended) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer;

a polycrystalline silicon plug overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug; and

a titanium layer overlying the etch stop layer and the polycrystalline silicon plug layer.

49. (Amended) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer;

a polycrystalline silicon plug overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug;

a titanium layer overlying the etch stop layer; and

a titanium silicide etch stop layer overlying the polycrystalline silicon plug layer.

50. (Amended) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

D3 cont

a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer;

a polycrystalline silicon plug overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug; and

a titanium silicide etch stop layer overlying the polycrystalline silicon plug layer.

51. (Amended) An intermediate in the manufacture of a semiconductor interconnect overlying a buried contact region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate

region and having a thickness selected such that the lowest upper surface of the first polycrystalline silicon layer is higher than the highest upper surface of the oxide region;

a polycrystalline silicon plug overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug; and

a titanium silicide etch stop layer overlying the polycrystalline silicon plug.

52. (Amended) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

D3 cont.

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer partially overlying the oxide region adjacent the first substrate region but not overlying the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

a polycrystalline silicon plug overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug; and

a titanium silicide etch stop layer overlying the polycrystalline silicon plug.

54. The intermediate of claim 38 wherein a portion of the second polycrystalline layer overlying the first polycrystalline layer is removed to expose the first polycrystalline layer and eliminate a horizontal interface between the first and second polycrystalline silicon layers.

55. The intermediate of claim 39 wherein a portion of the second polycrystalline silicon layer overlying the first polycrystalline layer is removed so that a total height of the first polycrystalline silicon layer plus a height of the etch stop layer defines a maximum height of the

second polycrystalline silicon layer after removal of the portion of the second polycrystalline silicon layer.

56. The intermediate of claim 40 wherein the first and second polycrystalline silicon layers are doped to increase their conductivity.

57. The intermediate of claim 56 wherein the first and second polycrystalline silicon layers are doped with arsenic.

58. The intermediate of claim 41 wherein the first and second polycrystalline silicon layers are doped to increase their conductivity.

59. The intermediate of claim 58 wherein the first and second polycrystalline silicon layers are doped with arsenic.

62. The intermediate of claim 44 wherein a photoresist mask is applied over a portion of the first etch stop layer and the second polycrystalline silicon layer.

63. The intermediate of claim 62 wherein a titanium layer is deposited to overlie the etch stop layer and the second polycrystalline silicon layer.

64. The intermediate of claim 45 wherein the polycrystalline plug and the polycrystalline silicon layer are doped to increase their conductivity.

65. The intermediate of claim 64 wherein the polycrystalline plug and the polycrystalline silicon layer are doped with arsenic.

68. The intermediate of claim 47 wherein the first and second polycrystalline silicon layers are doped to increase their conductivity.

69. The intermediate of claim 68 wherein the first and second polycrystalline silicon layers are doped with arsenic.

70. The intermediate of claim 48 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped to increase their conductivity.

71. The intermediate of claim 70 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped with arsenic.

72. The intermediate of claim 49 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped to increase their conductivity.

73. The intermediate of claim 72 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped with arsenic.

74. The intermediate of claim 50 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped to increase their conductivity.

75. The intermediate of claim 74 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped with arsenic.

76. The intermediate of claim 51 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped to increase their conductivity.

77. The intermediate of claim 76 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped with arsenic.

78. The intermediate of claim 52 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped to increase their conductivity.

79. The intermediate of claim 78 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped with arsenic.